Attorney Docket No. 0756-7839

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No.: 1460
Kiyoshi KATO	)	Group Art Unit: 2816
Serial No. 10/593,577	)	Examiner: Dinh Thanh Le
Filed: September 20, 2006	)	
For: LIMITER AND SEMICONDUCTOR DEVICE USING THE SAME	)	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. § 134 and 37 C.F.R. § 1.192(a), Appellants submit this Appeal Brief to appeal the examiner's final rejection of claims 1-28 in the Official Action mailed April 17, 2009. A Notice of Appeal was filed July 17, 2009.

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I. REAL PARTY IN INTEREST

The named inventors have assigned all ownership rights in the pending application to Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036, Japan, which is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

The appellants, their legal representatives, and the assignee are not aware of any other prior or pending appeals, interferences or judicial proceedings which will directly affect or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1-28 are pending in the present application, of which claims 1-6, 10 and 11 are independent. Claims 1-28 stand rejected. No claims have been deemed allowable by the examiner. The Appellants appeal the rejection of claims 1-28.

IV. STATUS OF AMENDMENTS

All prior amendments are believed to have been entered in the present application. A *Supplemental Response* has been filed concurrently herewith to request evidence of the Examiner's consideration of a citation in the Information Disclosure Statement filed September 4, 2008.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a semiconductor device (e.g. Embodiment 5, Figures 9-14, pages 24-44) comprising a limiter (e.g. 307, Figure 4A; 460, Figure 8; also Figures 1A, 5A-5C, 6A, 6B, 7 and 8), wherein the limiter includes: a transistor (e.g. 542, Figure 11C) including a semiconductor layer (e.g. 506, Figures 9-11), a floating gate (e.g. 515, Figures 10 and 11) and a control gate (e.g. 518, Figures 10 and 11), wherein the floating gate is formed over the semiconductor layer with a first insulating

film (e.g. 507, Figures 9-11) interposed therebetween; the floating gate and the control gate of the transistor overlap each other with a second insulating film (e.g. 509, Figures 9-11) interposed therebetween; a side surface of the floating gate is covered with a third insulating film (e.g. 530, Figure 11A); a drain of the transistor is connected to the control gate (e.g. Figure 11D); and the drain and the control gate are connected to an input terminal (e.g. Vin) and an output terminal (e.g. Vout), wherein the floating gate is electrically floating, and wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate (e.g. page 12, lines 19-22).

Independent claim 2 is directed to a semiconductor device (e.g. Embodiment 5, Figures 9-14, pages 24-44) comprising a limiter (e.g. 307, Figure 4A; 460, Figure 8; also Figures 1A, 5A-5C, 6A, 6B, 7 and 8), wherein the limiter includes: a transistor (e.g. 542, Figure 11C) including a semiconductor layer (e.g. 506, Figures 9-11), a floating gate (e.g. 515, Figures 10 and 11) and a control gate (e.g. 518, Figures 10 and 11), wherein the floating gate is formed over the semiconductor layer with a first insulating film (e.g. 507, Figures 9-11) interposed therebetween; the floating gate and the control gate of the transistor overlap each other with a second insulating film (e.g. 509, Figures 9-11) interposed therebetween; a side surface of the floating gate is covered with a third insulating film (e.g. 530, Figure 11A); a drain of the transistor is connected to the control gate (e.g. Figure 11D); and a source of the transistor is connected to an input terminal (e.g. Vin) and an output terminal (e.g. Vout), wherein the floating gate is electrically floating, and wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate (e.g. page 12, lines 19-22).

Independent claim 3 is directed to a semiconductor device (e.g. Embodiment 5, Figures 9-14, pages 24-44) comprising a limiter (e.g. 307, Figure 4A; 460, Figure 8; also Figures 1A, 5A-5C, 6A, 6B, 7 and 8), wherein the limiter includes: a plurality of transistors (e.g. 542, Figure 11C) each including a semiconductor layer (e.g. 506,

Figures 9-11), a floating gate (e.g. 515, Figures 10 and 11) and a control gate (e.g. 518, Figures 10 and 11), wherein the floating gate of each of the plurality of transistors is formed over the semiconductor layer of each of the plurality of transistors with a first insulating film (e.g. 507, Figures 9-11) interposed therebetween; the floating gate and the control gate of each of the plurality of transistors overlap each other with a second insulating film (e.g. 509, Figures 9-11) interposed therebetween; a side surface of the floating gate of each of the plurality of transistors is covered with a third insulating film (e.g. 530, Figure 11A); a drain of each of the plurality of transistors is connected to the control gate of each of the plurality of transistors (e.g. Figure 11D); the plurality of transistors are connected in series so as to have the same forward current direction (e.g. Figure 5A-5C, page 15, line 20, to page 16, line 28); and the drain and the control gate of one of the plurality of transistors are connected to an input terminal (e.g. Vin) and an output terminal (e.g. Vout), wherein the floating gate of each of the plurality of transistors is electrically floating, and wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate (e.g. page 12, lines 19-22).

Independent claim 4 is directed to a semiconductor device (e.g. Embodiment 5, Figures 9-14, pages 24-44) comprising a limiter (e.g. 307, Figure 4A; 460, Figure 8; also Figures 1A, 5A-5C, 6A, 6B, 7 and 8), wherein the limiter includes: a plurality of transistors (e.g. 542, Figure 11C) each including a semiconductor layer (e.g. 506, Figures 9-11), a floating gate (e.g. 515, Figures 10 and 11) and a control gate (e.g. 518, Figures 10 and 11), wherein the floating gate of each of the plurality of transistors is formed over the semiconductor layer of each of the plurality of transistors with a first insulating film (e.g. 507, Figures 9-11) interposed therebetween; the floating gate and the control gate of each of the plurality of transistors overlap each other with a second insulating film (e.g. 509, Figures 9-11) interposed therebetween; a side surface of the floating gate of each of the plurality of transistors is covered with a third insulating film (e.g. 530, Figure 11A); a drain of each of the plurality of transistors is connected to the

control gate of each of the plurality of transistors (e.g. Figure 11D); the plurality of transistors are connected in series so as to have the same forward current direction (e.g. Figure 5A-5C, page 15, line 20, to page 16, line 28); and a source of one of the plurality of transistors is connected to an input terminal (e.g. Vin) and an output terminal (e.g. Vout), wherein the floating gate of each of the plurality of transistors is electrically floating, and wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate (e.g. page 12, lines 19-22).

Independent claim 5 is directed to a semiconductor device (e.g. Embodiment 5, Figures 9-14, pages 24-44) comprising a limiter (e.g. 307, Figure 4A; 460, Figure 8; also Figures 1A, 5A-5C, 6A, 6B, 7 and 8), wherein the limiter includes: a first transistor (e.g. 402/403, Figure 5A; 413, Figure 5B; 422, Figure 5C; 466, Figure 8), and a second transistor (e.g. 403/402, Figure 5A; 412, Figure 5B; 423, Figure 5C; 467, Figure 8), wherein a floating gate (e.g. 515, Figures 10 and 11) of the first transistor is formed over a semiconductor layer (e.g. 506, Figures 9-11) of the first transistor with a first insulating film (e.g. 507, Figures 9-11) interposed therebetween; the floating gate and a control gate (e.g. 518, Figures 10 and 11) of the first transistor overlap each other with a second insulating film (e.g. 509, Figures 9-11) interposed therebetween; a side surface of the floating gate of the first transistor is covered with a third insulating film (e.g. 530, Figure 11A); a drain of the first transistor is connected to the control gate of the first transistor (e.g. Figures 5A, 5B, 5C, 8 and 11D); a drain of the second transistor is connected to a gate of the second transistor (e.g. Figures 5A, 5B, 5C and 8); the first transistor and the second transistor are connected in series so as to have the same forward current direction (e.g. Figure 5A-5C, page 15, line 20, to page 16, line 28); and the drain of the second transistor and the control gate are connected to an input terminal (e.g. Vin) and an output terminal (e.g. Vout), wherein the floating gate of the first transistor is electrically floating, and wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate (e.g. page 12, lines 19-22).

Independent claim 6 is directed to a semiconductor device (e.g. Embodiment 5, Figures 9-14, pages 24-44) comprising a limiter (e.g. 307, Figure 4A; 460, Figure 8; also Figures 1A, 5A-5C, 6A, 6B, 7 and 8), wherein the limiter includes: a first transistor (e.g. 402/403, Figure 5A; 413, Figure 5B; 422, Figure 5C; 466, Figure 8), and a second transistor (e.g. 403/402, Figure 5A; 412, Figure 5B; 423, Figure 5C; 467, Figure 8), wherein a floating gate (e.g. 515, Figures 10 and 11) of the first transistor is formed over a semiconductor layer (e.g. 506, Figures 9-11) of the first transistor with a first insulating film (e.g. 507, Figures 9-11) interposed therebetween; the floating gate and a control gate (e.g. 518, Figures 10 and 11) of the first transistor overlap each other with a second insulating film (e.g. 509, Figures 9-11) interposed therebetween; a side surface of the floating gate of the first transistor is covered with a third insulating film (e.g. 530, Figure 11A); a drain of the first transistor is connected to the control gate of the first transistor (e.g. Figures 5A, 5B, 5C, 8 and 11D); a drain of the second transistor is connected to a gate of the second transistor (e.g. Figures 5A, 5B, 5C and 8); the first transistor and the second transistor are connected in series so as to have the same forward current direction (e.g. Figure 5A-5C, page 15, line 20, to page 16, line 28); and a source of the second transistor is connected to an input terminal (e.g. Vin) and an output terminal (e.g. Vout), wherein the floating gate of the first transistor is electrically floating, and wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate (e.g. page 12, lines 19-22).

Independent claim 10 is directed to a semiconductor device (e.g. Embodiment 5, Figures 9-14, pages 24-44) comprising: an integrated circuit (e.g. 201, Figure 3A; 205, Figure 3B; 301, Figures 4A and 4B; 1211/1213, Figure 16B; 601, Figures 17A and 17C), and an antenna (e.g. 202, Figure 3A; 206, Figure 3B; 302, Figures 4A and 4B; 1206, Figure 16A; 602, Figures 17A and 17C) connected to the integrated circuit, wherein the integrated circuit includes a limiter (e.g. 307, Figure 4A; 460, Figure 8; also Figures 1A, 5A-5C, 6A, 6B, 7 and 8); the limiter includes a transistor (e.g. 542, Figure 11C); a floating gate (e.g. 515, Figures 10 and 11) of the transistor is formed over a

semiconductor layer (e.g. 506, Figures 9-11) of the transistor with a first insulating film (e.g. 507, Figures 9-11) interposed therebetween; the floating gate and a control gate (e.g. 518, Figures 10 and 11) of the transistor overlap each other with a second insulating film (e.g. 509, Figures 9-11) interposed therebetween; a side surface of the floating gate is covered with a third insulating film (e.g. 530, Figure 11A); a drain of the transistor is connected to the control gate (e.g. Figure 11D); and the drain and the control gate are connected to an input terminal (e.g. Vin) and an output terminal (e.g. Vout), wherein the floating gate is electrically floating, and wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate (e.g. page 12, lines 19-22).

Independent claim 11 is directed to a semiconductor device (e.g. Embodiment 5, Figures 9-14, pages 24-44) comprising an integrated circuit (e.g. 201, Figure 3A; 205, Figure 3B; 301, Figures 4A and 4B; 1211/1213, Figure 16B; 601, Figures 17A and 17C) and an antenna (e.g. 202, Figure 3A; 206, Figure 3B; 302, Figures 4A and 4B; 1206, Figure 16A; 602, Figures 17A and 17C) connected to the integrated circuit, wherein the integrated circuit includes a limiter (e.g. 307, Figure 4A; 460, Figure 8; also Figures 1A, 5A-5C, 6A, 6B, 7 and 8), a pulse generation circuit (e.g. 463, Figure 8) for controlling a limit voltage of the limiter, and a booster circuit (e.g. 464, Figure 8) for supplying a power supply voltage to the pulse generation circuit; the limiter includes a transistor (e.g. 542, Figure 11C); a floating gate (e.g. 515, Figures 10 and 11) of the transistor is formed over a semiconductor layer (e.g. 506, Figures 9-11) of the transistor with a first insulating film (e.g. 507, Figures 9-11) interposed therebetween; the floating gate and a control gate (e.g. 518, Figures 10 and 11) of the transistor overlap each other with a second insulating film (e.g. 509, Figures 9-11) interposed therebetween; a side surface of the floating gate is covered with a third insulating film (e.g. 530, Figure 11A); a drain of the transistor is connected to the control gate (e.g. Figure 11D); and the drain and the control gate are connected to an input terminal (e.g. Vin) and an output terminal (e.g. Vout), wherein the floating gate is electrically floating, and wherein the limiter is

configured to change the limit voltage by controlling an amount of charge accumulated in the floating gate (e.g. page 12, lines 19-22).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1-28 are indefinite under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

B. Whether claims 1-28 are obvious under 35 U.S.C. § 103 based on the alleged combination of U.S. Patent No. 6,670,679 to Hirata and U.S. Patent No. 6,300,656 to Ueno. The rejected claims shall stand or fall together.

VII. ARGUMENTS

A. Whether claims 1-28 are indefinite under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Official Action rejects claims 1-28 under 35 U.S.C. § 112, second paragraph, asserting that the claims are "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention" (page 2, Paper No. 20090415). Specifically, the Official Action argues "it is unclear what the 'limit voltage' on line 14 is, where the voltage and the charge on line 14 come from, how the voltage can be 'changed', and [how] the charge can be accumulated and controlled since no means for performing the controlling function is recited" (Id.). The Appellant respectfully disagrees and traverses the assertions in the Official Action.

MPEP § 2173.04, Breadth Is Not Indefiniteness, sets forth the following: "Breadth of a claim is not to be equated with indefiniteness. In re Miller, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different from that defined in the claims, then the claims comply with 35 U.S.C. 112, second paragraph."

The Appellant notes that the Official Action has not questioned support for the claim features, and that the claims must be read in light of the specification. In this case, the Official Action seems to be specifically concerned with the recitation of "a limit voltage" and asserts that it is not clear where the voltage and the charge come from and how the charge can be changed. However, the present specification is clear in describing the limit voltage itself and how the limit voltage can be changed or controlled. In the *Amendment* filed February 5, 2009, the Appellant amended the independent claims to recite that a limiter is configured to change a limit voltage by controlling an amount of charge accumulated in a floating gate and cited, as a statement of support, page 12, lines 19-22. However, the support for these features is not limited to page 12, liens 19-22. As noted at page 3, lines 10-12, "the invention provides a limiter capable of controlling a limit voltage with accuracy" and "[t]he invention also provides a semiconductor device capable of controlling a limit voltage with accuracy." See also, e.g., the detailed descriptions in the present specification as follows: page 2, line 3, to page 3, line 15; page 5, lines 15-23; page 8, lines 18-22; page 10, lines 2-9; page 11, lines 17-22; page 12, line 16, to page 13, line 2 (Figure 21); page 14, line 5, to page 15, line 4; page 16, lines 5-7; page 16, line 29, to page 17, line 1; page 17, lines 23-26; page 18, lines 21-23; and page 22, line 11, to page 24, line 1.

The Appellant respectfully submits that the present specification is clear as to the claimed "limit voltage." Therefore, claims 1-28 particularly point out and distinctly claim the subject matter which applicant regards as the invention and are definite.

Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 112 are in order and respectfully requested.

B. Whether claims 1-28 are obvious under 35 U.S.C. § 103 based on the alleged combination of U.S. Patent No. 6,670,679 to Hirata and U.S. Patent No. 6,300,656 to Ueno.

The Official Action rejects claims 1-28 as obvious based on the combination of U.S. Patent No. 6,670,679 to Hirata and U.S. Patent No. 6,300,656 to Ueno. The Appellant respectfully traverses the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2144.04, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some reason to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

There is no proper or sufficient reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Hirata and

Ueno or to combine reference teachings to achieve the claimed invention. MPEP § 2142 states that the examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. It is respectfully submitted that the Official Action has failed to carry this burden. While the Official Action relies on various teachings of the cited prior art to disclose aspects of the claimed invention and asserts that these aspects could be modified in the manner asserted in the Official Action, it is submitted that the Official Action does not adequately set forth why one of skill in the art would combine the references to achieve the features of the present invention.

Independent claims 1-6, 10 and 11 recite that a floating gate is electrically floating. The Official Action asserts that Hirata teaches "a floating gate (106, 106a in Figure 10 or 55 in Figure 12A)" (page 3, Paper No. 20090415). Although Hirata describes a "floating" gate, it is important to note (as described in greater detail below), that Hirata's "floating" gate is not electrically floating.

Indeed, the Official Action concedes that "Hirata does not disclose that ... the floating gate is electrically floated" (Id.) and relies on Ueno to allegedly cure these deficiencies in Hirata (pages 3-4, Id.). The Official Action asserts that it would have been obvious to make the floating gate 106, 106a or 55 of Hirata electrically floating based on the floating gate 4 of Figure 1 of Ueno.

The Official Action asserts that "[i]t would have been obvious ... to form the MOS transistor of Hirata as suggested by Ueno et al for the purpose of reducing a longitudinal electric field ... so as to increase a probability with which generated high energy electrons are injected into a floating gate electrode" (page 4, Paper No. 20090415). The Applicant respectfully disagrees and traverses the assertions in the Official Action.

The Appellant respectfully submits that the floating gate electrode 106, 106a or 55 of Hirata is connected to a source line or ground (see Figures 4-7 and 9-12, particularly Figures 10 and 12A, reproduced and annotated below, arrows have been

added to show the electrical connection of the gate electrode to a resistor and a ground line).

FIG. 10

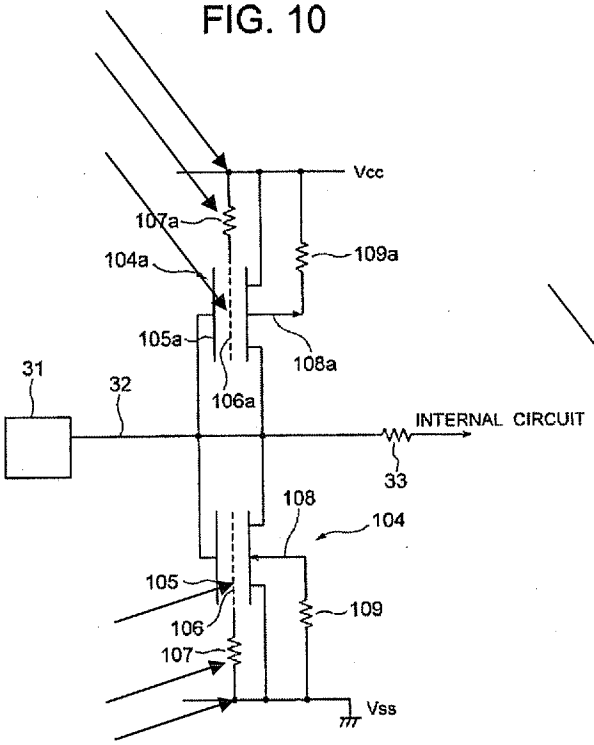
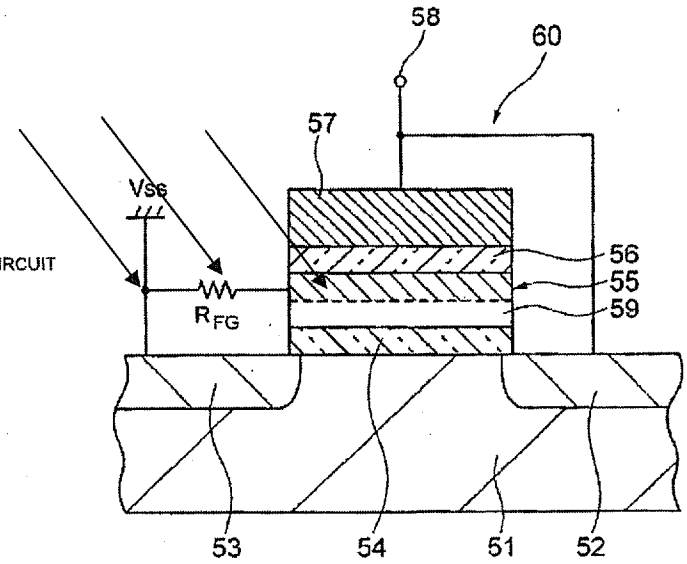


FIG. 12A



As such, it is clear that Hirata's floating gate electrode is not electrically floating.

The connection of the floating gate electrode to a source line or ground is an essential limitation of Hirata's invention. See Summary of the Invention, column 4, lines 5-24. Hirata appears to have as its intended function a protective circuit having a "floating gate connected to the constant potential line or a first line" (column 4, lines 13-14) or "a floating gate connected to a ground line" (column 4, lines 23-24). Indeed, Hirata teaches "a floating gate 106 connected to the ground line VSS via a floating gate resistor 107" (column 5, lines 34-37). The resistor 107 is a crucial point of the Hirata's invention since "[t]he peak voltage ΔV_{FG} and the rise period of the momentary potential rise of the floating gate 106 are determined by the capacitances of the inter-electrode insulation film and the tunnel oxide film as well as the resistance of the floating gate resistor 107" (column 6, lines 41-46). As such, any modification of Hirata's floating gate

that would involve removing the electrical connections between the floating gate and the resistor or the ground line would be contrary to Hirata's intended function.

Ueno does not cure the deficiencies in Hirata. The Official Action acknowledges that "Hirata does not disclose that a side surface of the floating gate is covered with a third insulation film, the floating gate is electrically floated and controlled and a plurality of transistors are connected in series so as to have the same forward current direction" (page 3, Paper No. 20090415). The Official Action relies on Ueno to allegedly teach that "a MOS transistor is formed with a floating gate (4), a control gate (6), insulating films (3, 5), and a third insulating film (7) covering sides surface of the floating gate (4)" (Id.). However, Ueno does not teach or suggest why one of ordinary skill in the art at the time of the present invention would have had any reason to modify Hirata's floating gate electrode so that it would no longer be connected to a source line or ground. In contrast with Hirata, where a floating gate is connected to a ground line V_{SS} via a floating gate resistor, the floating gate described by Ueno is insulated and made to be electrically floating in order to fulfill its function, i.e. that of a permanent memory element (see, e.g., column 2, lines 46-58).

Furthermore, the proposed modification of Hirata in view of Ueno would appear to render Hirata unsatisfactory for its intended purpose and change the principle of operation of Hirata, which are contrary to obviousness. As noted in MPEP § 2143.01, Part V, if a proposed modification renders the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Also, as noted in MPEP § 2143.01, Part VI, if a proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). The Official Action appears to propose modifying Hirata's floating gate electrode so that it is no longer connected to a source line or ground. The Official Action cites

Ueno's floating gate electrodes 4 as evidence that such modification would be obvious. However, the proposed modification would render Hirata unsatisfactory for its intended function of providing a protective circuit, as stated above, and Ueno does not explain why one would modify Hirata in a manner contrary to its intended function in order to achieve the features of the present invention.

In the "Response to Applicant's Arguments" in the Official Action mailed November 5, 2008, the Examiner argued that "the modified circuit of Hirata in view of Ueno would provide the structure of the claimed circuit" and that this modified device "would perform the same function as the claimed circuit" (pages 5-6, Paper No. 20081104). This argument misses the point, i.e. that one of ordinary skill in the art at the time of the present invention would not have had a reason to modify Hirata in a manner that would change its underlying function or change its principle of operation.

The statements of alleged motivation do not address the fact that the proposed modification would render Hirata unsatisfactory for its intended purpose and change the principle of operation of Hirata. The Official Action asserts that "[i]t would have been obvious ... to form the MOS transistor of Hirata as suggested by Ueno et al for the purpose of reducing a longitudinal electric field ... so as to increase a probability with which generated high energy electrons are injected into a floating gate electrode" (page 4, Paper No. 20090415). Also, the Official Action asserts that "[i]t would have been obvious ... to control the floating gate of Hirata for the purpose of controlling the limit voltage, and employ a plurality of diode connected transistors as claimed or the purpose of increasing voltage drops and accommodating with the requirement of a predetermined system" (Id.). However, these statements, aside from having no apparent support in the prior art of record, do not explain why one of ordinary skill in the art at the time of the present invention would have had any reason to modify a device, such as Hirata, so that Hirata's floating gate electrode would no longer be connected to a source line or ground, or why one of ordinary skill in the art at the time of the present

invention would have had a reason to modify Hirata in a manner that would change its underlying function and change its principle of operation.

Since the Examiner's proposed modification or combination of the prior art appears to change the principle of operation of the prior art invention being modified and changes the principle of operation of Hirata, the Appellant respectfully submits that there is no suggestion or motivation to make the proposed modification, and the teachings of the references are not sufficient to render the claims *prima facie* obvious.

Therefore, the Appellant respectfully submits that the Official Action has not provided a proper or sufficient reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Hirata and Ueno or to combine reference teachings to achieve the claimed invention.

In the present application, it is respectfully submitted that the prior art of record, either alone or in combination, does not expressly or impliedly suggest the claimed invention and the Official Action has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

For the reasons stated above, the Official Action has not formed a proper *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

For all of the above reasons, it is respectfully asserted that the pending claims of the present application are unobvious in view of the prior art of record. Reversal of the outstanding rejections of record and allowance of the claims of this application is requested. If the Examiner feels further discussions would expedite prosecution of this application, the Examiner is invited to contact the undersigned.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

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VIII. APPENDICES

A. CLAIMS INVOLVED IN THE APPEAL 19

B. REFERENCES OF RECORD 30

1. U.S. Patent No. 6,670,679 to Hirata

2. U.S. Patent No. 6,300,656 to Ueno

C. EVIDENCE APPENDIX 30

D. RELATED PROCEEDINGS APPENDIX 30

APPENDIX A

PENDING CLAIMS

1. (Previously Presented) A semiconductor device comprising a limiter,

wherein the limiter includes:

a transistor including a semiconductor layer, a floating gate and a control gate,

wherein the floating gate is formed over the semiconductor layer with a first insulating film interposed therebetween;

the floating gate and the control gate of the transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate is covered with a third insulating film;

a drain of the transistor is connected to the control gate; and

the drain and the control gate are connected to an input terminal and an output terminal,

wherein the floating gate is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

2. (Previously Presented) A semiconductor device comprising a limiter,

wherein the limiter includes:

a transistor including a semiconductor layer, a floating gate and a control gate,

wherein the floating gate is formed over the semiconductor layer with a first

insulating film interposed therebetween;

the floating gate and the control gate of the transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate is covered with a third insulating film;

a drain of the transistor is connected to the control gate; and

a source of the transistor is connected to an input terminal and an output terminal,

wherein the floating gate is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

3. (Previously Presented) A semiconductor device comprising a limiter,

wherein the limiter includes:

a plurality of transistors each including a semiconductor layer, a floating gate and a control gate,

wherein the floating gate of each of the plurality of transistors is formed over the semiconductor layer of each of the plurality of transistors with a first insulating film interposed therebetween;

the floating gate and the control gate of each of the plurality of transistors overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate of each of the plurality of transistors is covered

with a third insulating film;

a drain of each of the plurality of transistors is connected to the control gate of each of the plurality of transistors;

the plurality of transistors are connected in series so as to have the same forward current direction; and

the drain and the control gate of one of the plurality of transistors are connected to an input terminal and an output terminal,

wherein the floating gate of each of the plurality of transistors is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

4. (Previously Presented) A semiconductor device comprising a limiter,

wherein the limiter includes:

a plurality of transistors each including a semiconductor layer, a floating gate and a control gate,

wherein the floating gate of each of the plurality of transistors is formed over the semiconductor layer of each of the plurality of transistors with a first insulating film interposed therebetween;

the floating gate and the control gate of each of the plurality of transistors overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate of each of the plurality of transistors is covered with a third insulating film;

a drain of each of the plurality of transistors is connected to the control gate of each of the plurality of transistors;

the plurality of transistors are connected in series so as to have the same forward current direction; and

a source of one of the plurality of transistors is connected to an input terminal and an output terminal,

wherein the floating gate of each of the plurality of transistors is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

5. (Previously Presented) A semiconductor device comprising a limiter,

wherein the limiter includes:

a first transistor, and

a second transistor,

wherein a floating gate of the first transistor is formed over a semiconductor layer of the first transistor with a first insulating film interposed therebetween;

the floating gate and a control gate of the first transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate of the first transistor is covered with a third insulating film;

a drain of the first transistor is connected to the control gate of the first transistor;

a drain of the second transistor is connected to a gate of the second transistor;

the first transistor and the second transistor are connected in series so as to have the same forward current direction; and

the drain of the second transistor and the control gate are connected to an input terminal and an output terminal,

wherein the floating gate of the first transistor is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

6. (Previously Presented) A semiconductor device comprising a limiter,

wherein the limiter includes:

a first transistor, and

a second transistor,

wherein a floating gate of the first transistor is formed over a semiconductor layer of the first transistor with a first insulating film interposed therebetween;

the floating gate and a control gate of the first transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate of the first transistor is covered with a third

insulating film;

a drain of the first transistor is connected to the control gate of the first transistor;

a drain of the second transistor is connected to a gate of the second transistor;

the first transistor and the second transistor are connected in series so as to have the same forward current direction; and

a source of the second transistor is connected to an input terminal and an output terminal,

wherein the floating gate of the first transistor is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

7. (Previously Presented) The semiconductor device according to claim 1 further comprising a connecting terminal, wherein the connecting terminal is connected to the drain of the transistor.

8. (Previously Presented) The semiconductor device according to claim 1 further comprising a resistor, wherein the drain of the transistor is connected to the input terminal through the resistor.

9. (Previously Presented) The semiconductor device according to claim 1, wherein the transistor is a thin film transistor.

10. (Previously Presented) A semiconductor device comprising:

an integrated circuit, and

an antenna connected to the integrated circuit,

wherein the integrated circuit includes a limiter;

the limiter includes a transistor;

a floating gate of the transistor is formed over a semiconductor layer of the transistor with a first insulating film interposed therebetween;

the floating gate and a control gate of the transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate is covered with a third insulating film;

a drain of the transistor is connected to the control gate; and

the drain and the control gate are connected to an input terminal and an output terminal,

wherein the floating gate is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

11. (Previously Presented) A semiconductor device comprising an integrated circuit and an antenna connected to the integrated circuit,

wherein the integrated circuit includes a limiter, a pulse generation circuit for

controlling a limit voltage of the limiter, and a booster circuit for supplying a power supply voltage to the pulse generation circuit;

the limiter includes a transistor;

a floating gate of the transistor is formed over a semiconductor layer of the transistor with a first insulating film interposed therebetween;

the floating gate and a control gate of the transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate is covered with a third insulating film;

a drain of the transistor is connected to the control gate; and

the drain and the control gate are connected to an input terminal and an output terminal,

wherein the floating gate is electrically floating, and

wherein the limiter is configured to change the limit voltage by controlling an amount of charge accumulated in the floating gate.

12. (Original) The semiconductor device according to claim 10 or 11, wherein the transistor is a thin film transistor.

13. (Previously Presented) The semiconductor device according to claim 10 or 11 further comprising a resistor, wherein the drain of the transistor is connected to the input terminal through the resistor.

14. (Previously Presented) The semiconductor device according to claim 2 further comprising a connecting terminal, wherein the connecting terminal is connected to the source of the transistor.

15. (Previously Presented) The semiconductor device according to claim 3 further comprising a connecting terminal, wherein the connecting terminal is connected to the drain of the one of the plurality of transistors.

16. (Previously Presented) The semiconductor device according to claim 4 further comprising a connecting terminal, wherein the connecting terminal is connected to the source of the one of the plurality of transistors.

17. (Previously Presented) The semiconductor device according to claim 5 further comprising a connecting terminal, wherein the connecting terminal is connected to the drain of the second transistor.

18. (Previously Presented) The semiconductor device according to claim 6 further comprising a connecting terminal, wherein the connecting terminal is connected to the source of the second transistor.

19. (Previously Presented) The semiconductor device according to claim 2 further comprising a resistor, wherein the source of the transistor is connected to the input terminal through the resistor.

20. (Previously Presented) The semiconductor device according to claim 3 further comprising a resistor, wherein the drain of the one of the plurality of transistors is connected to the input terminal through the resistor.

21. (Previously Presented) The semiconductor device according to claim 4 further comprising a resistor, wherein the source of the one of the plurality of transistors is connected to the input terminal through the resistor.

22. (Previously Presented) The semiconductor device according to claim 5 further comprising a resistor, wherein the drain of the second transistor is connected to the input terminal through the resistor.

23. (Previously Presented) The semiconductor device according to claim 6 further comprising a resistor, wherein the source of the second transistor is connected to the input terminal through the resistor.

24. (Previously Presented) The semiconductor device according to claim 2,

wherein the transistor is a thin film transistor.

25. (Previously Presented) The semiconductor device according to claim 3, wherein the plurality of transistors are thin film transistors.

26. (Previously Presented) The semiconductor device according to claim 4, wherein the plurality of transistors are thin film transistors.

27. (Previously Presented) The semiconductor device according to claim 5, wherein the second transistor is a thin film transistor.

28. (Previously Presented) The semiconductor device according to claim 6, wherein the second transistor is a thin film transistor.

APPENDIX B
REFERENCES

Copies attached.

APPENDIX C
EVIDENCE APPENDIX

Not applicable.

APPENDIX D
RELATED PROCCEDINGS APPENDIX

Not applicable.